CL1026

24bit Ultralow Power Stereo Mobile CODEC with MIC and HP

1. General Description

The CL1026 features a flexible clocking architecture, allowing the device to use reference clock frequencies of 6, 6.144,12 or 12.288 MHz, or any standard audio master clock. One asynchronous bidirectional serial ports support multiple clock domains. One asynchronous sample rate converters synchronize and convert the audio samples to the internal processing rate. A stereo mic input is routed to a PGA then to a stereo ADC. The mic inputs has +12 or +18 dB gain. Two independent, low-noise mic bias voltage supplies are also provided. Either the stereo ADC or a digital mic interface output is selected to be decimated, selectively DC highpass filtered, selectively 5 Band BiQuad Equalized, channel-swapped or mono-to-stereo routed, wind noise filtered and volume adjusted or muted. The volume levels can be automatically adjusted via a programmable ALC and noise gate. A digital mixer is used to mix and route the CL1026's inputs (analog inputs to ADC, digital mic, or serial ports) to outputs (DAC-fed amplifiers or serial ports). Each mixer input has independent attenuation. Volume adjustment and mute control is applied to the output paths from the digital mixer to the two stereo DACs. A peak-detector can be used to automatically adjust the volume levels via a programmable limiter. The stereo DAC feeds the stereo headphone output amplifiers, which are powered from a dedicated positive supply. 5 band BiQuad Equalizer supply different sound colors. An integrated charge pump provides a negative supply. This allows a ground-centered analog output with a wide signal swing, and eliminates external DC-blocking capacitors while reducing pops and clicks. Bi-level Class H amplification is used to reduce power consumption under low-signal-level conditions. Analog volume controls are provided on the stereo headphone outputs. A high-speed I2C control port interface capable of up to 400 kHz operation facilitates register programming.The CL1026 is available in 40L QFN5x5 packages for the commercial (-30° to +85° C) grade

2. Applications

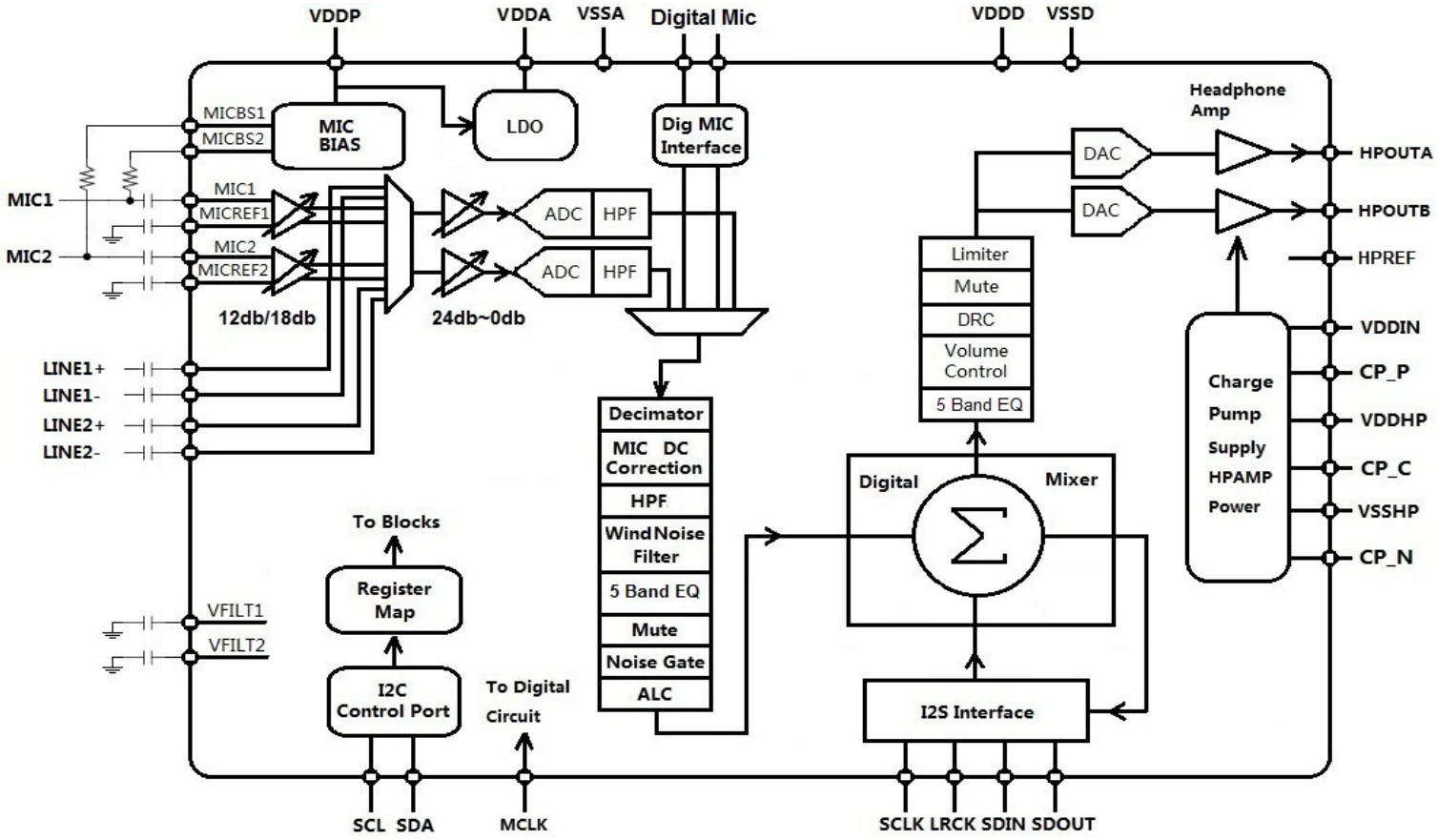
- **Digital Mic and Headphone**
- **Wireless IP camera**
- **Mobile Internet Devices**
- **Car Driving Camera**

3. Features

- **Native (no PLL required) support for 6/6.144/12/12.288 MHz master clock rates**
- **High-efficiency power management reduces power consumption – Charge pump provides low supply voltage and negative voltage for HP amplifier**
- **Individual power-down controls for ADCs, digital mic, micbias generators, serial ports, and output amplifiers and associated DACs**
- **Line In and ADC 100db SNR (A-weighted) with 1.1 Vrms Input, 100db Dynamic Range (A-weighted)**
- **Line In and ADC -96 dB THD+N**

- MIC preamp(12db Gain) and ADC 95db SNR (A-weighted), 100db Dynamic Range (A-weighted)
- MIC preamp(12db Gain) and ADC -92 dB THD+N
- Dual analog mic inputs, two independent programmable low-noise mic bias outputs
- Analog MIC gain boost 12 dB or 18 dB
- Analog programmable gain amplifier (PGA) (0dB to 24db in 1 dB steps)
- Programmable automatic level control (ALC), Noise gate for noise suppression
- Wind Noise Filter for noise suppression
- Programmable digital microphone clock rate: Integer divide by 2 or 4 of internal MCLK
- DAC and Headphone 104dB SNR (A-weighted)
- DAC and Headphone -95 dB THD+N with 3K ohms load, -94 dB THD+N with 32 ohms load
- Fully custom 5 Band BiQuad Equalizer for record path or playback path
- Danymic Range Compression for playback path
- Class H amplifier, automatic supply adjustment, High efficiency, Low EMI
- Headphone Pseudodifferential ground-centered outputs
- High HP power output 2 x 50mW into 16 ohms headphone @ 1.8 V
- Pop and click suppression
- Headphone Analog volume control (+6 to -54 dB in 2 dB steps) with zero-cross transitions
- Headphone Digital volume control (+12 to -102 dB in 0.5 dB steps) with soft-ramp transitions
- Programmable peak-detect and limiter
- I²S interface master or slave operation
- 8, 11.025, 12, 16, 22.05, 24, 32, 44.10, and 48 kHz sample rates
- Asynchronous sample rate converters

4. Block Diagram



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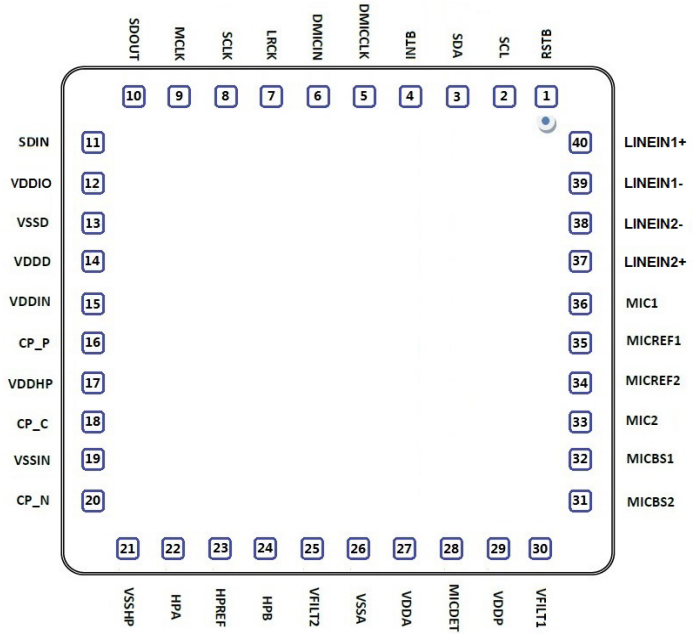
6. PACKAGE AND CONFIGURATIONS



6. 1 Pin Descriptions

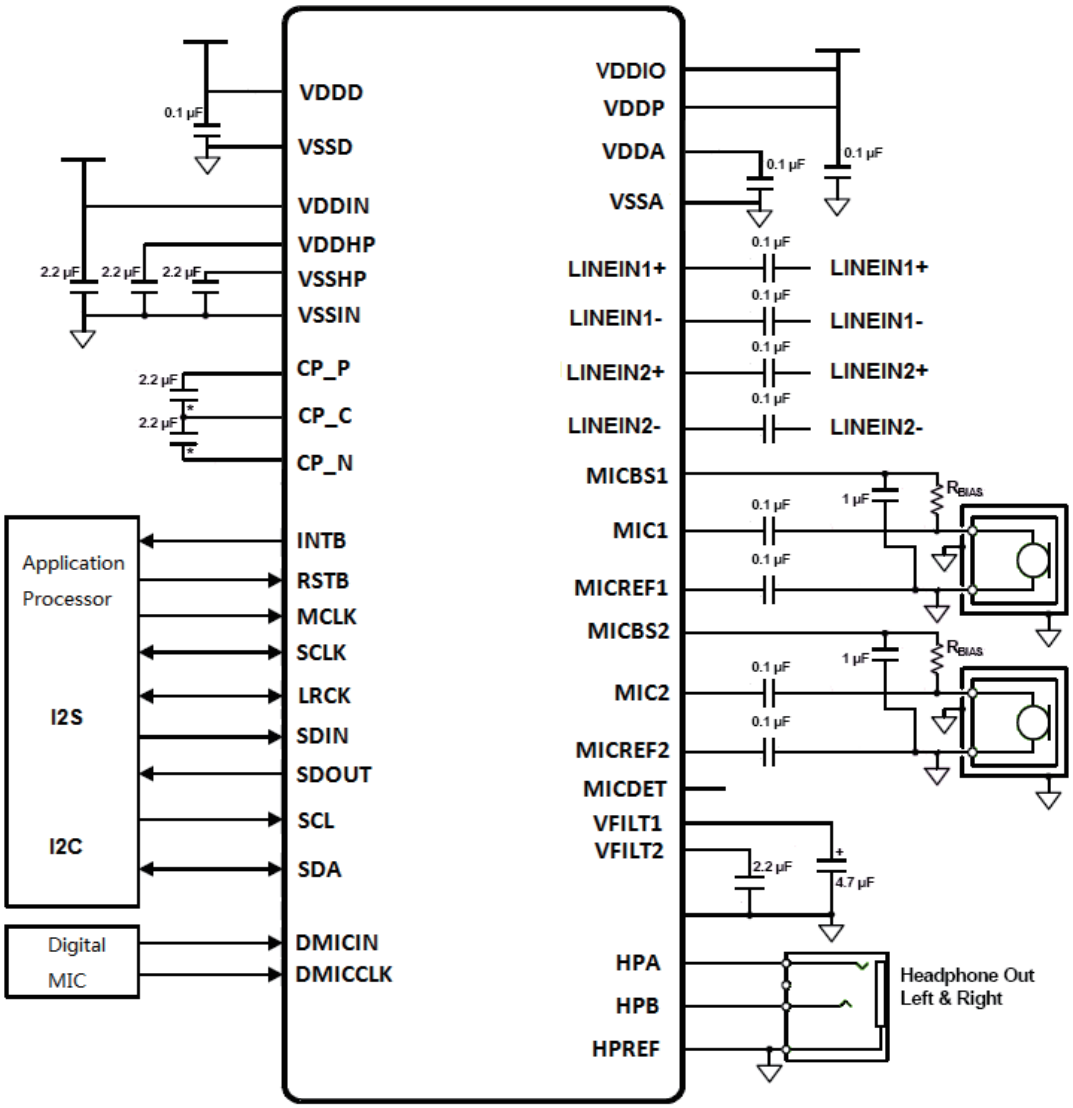
MCLK	Clock (Input).
INTB	Interrupt Request (Output). Open-drain active low.
RSTB	Reset (Input). The device enters a low-power mode when this pin is low.
SCL	Serial Control Port Clock (Input). I²C Serial clock. (Pin #1)
SDA	Serial Control Data (Input/Output). SDA is I²C bidirectional data pin.
MIC1/2	Microphone Inputs 1 and 2 (Input).
MICREF1/2	Microphone Inputs 1 and 2 Pseudodifferential References (Input).
LINEIN1/2+	Line Input 1+ and 2+ (Input).
LINEIN1/2-	Line Input 1- and 2- (Input).
MICBS1/2	Microphone Bias Voltages 1 and 2 (Output). Bias voltage for the MIC1/2
MICDET	Microphone 2 Short Detect (Input).
DMICCLK	Digital Mic Serial Clock (Output). Clock output to the digital microphone(s).
DMICIN	Digital Mic Serial Data (Input). Digital microphone data input.
SCLK	I2S Serial Clock (Input/Output). Serial shift clock for the interface.
LRCK	I2S Left/Right Clock (Input/Output). Indicates which channel, Left or Right, is currently active.
SDIN	I2S Data Input (Input). Input for two's complement serial audio data.
SDOUT	I2S Data Output (Output). Output for serial audio data.
HPA/B	Headphone Audio Output (Output).
HPREF	Pseudodifferential Headphone Output Reference (Input). Ground reference for the headphone.
VDDD	Digital Interface/Core Power (Input). Digital core logic power supply.
VSSD	Digital Ground (Input). Ground reference for the internal digital section.
VDDIN	Charge Pump Power (Input). Power supply for charge pump.
VDDIO	Digital I/O port power supply.
VDDHP	Charge Pump Filter Connection (Output). Power supply from charge pump that provides the positive rail for the headphone amplifiers.
VSSHP	Inverting Charge Pump Filter Connection (Output). Negative Voltage from charge pump for the headphone amplifiers.
CP_P	Charge Pump Cap Positive Node (Output).
CP_C	Charge Pump Cap Ground (Output).
CP_N	Charge Pump Cap Negative Node (Output).
VSSIN	Charge Pump Ground (Input). Ground reference for the internal headphone amplifiers.
VFILT1	Microphone Bias Source Voltage Filter (Output). Filter for MICBIAS.
VFILT2	Positive Voltage Reference (Output). Positive reference voltage for the internal sampling circuits.
VDDA	Analog Power (Input). Power supply for the internal analog section.
VDDP	MIC BIAS Power (Input). Power supply for the mic bias generators.
VSSA	Analog Ground (Input). Ground reference for the internal analog section.

6. 2 Digital Pin I/O Configurations

Power Supply	I/O Name	Internal Connections	Configuration
VDDIO	MCLK	Weak Pull-down	Hysteresis on CMOS Input
	RSTB	-	Hysteresis on CMOS Input
	SCL	-	Hysteresis on CMOS Input
	SDA	-	Hysteresis on CMOS Input/ CMOS Open-drain Output
	$\overline{INT}$	Weak Pull-up	CMOS Open-drain Output
	SCLK	Weak Pull-down	Hysteresis on CMOS Input/ CMOS Output
	LRCK	Weak Pull-down	Hysteresis on CMOS Input/CMOS Output
	SDIN	Weak Pull-down	Hysteresis on CMOS Input
	SDOUT	Weak Pull-down	Tristateable CMOS Output
	DMICCLK	-	CMOS Output
	DMICIN	Weak Pull-down	Hysteresis on CMOS Input

Notes: All outputs are disabled when RESET is active.

7. TYPICAL CONNECTION DIAGRAM



STEREO-ADC AND DUAL-DIGITAL-MIC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Fs = 48 kHz (Note 10), fDMIC_SCLK = 3.072 MHz

Parameters	Typ	Units
Low-Pass Filter Characteristics		
Frequency Response (20 Hz to 20 kHz)	+/- 0.2	dB
Passband to -0.05 dB corner	0.41	Fs
Passband to -3.0 dB corne	0.49	Fs
Stopband	0.60	Fs
Stopband Attenuation	33	dB
Total Input Path Digital Filter Group Delay	4.3/Fs	Fs
High-Pass Filter Characteristics		
Passband to -3.0 dB corner	4x10-5	Fs
Passband to -0.05 dB corner	3.5x10-4	Fs
Passband Ripple	0.01	dB

MIC BIAS CHARACTERISTICS

Test Conditions: Connections to the CL1026 are shown in the “Typical Connection Diagram”; VSSD = VSSA = VSSIN = 0 V; VA = 1.80 V, VP = 3.30 V; TA = +25 C; IOUT = 500 µA; only one bias output is powered up at a time; MIC_BIAS_CTRL = 1b.

Parameters		Typ	Units
MIC1_BIAS and MIC2_BIAS Characteristics		2.00	V
Output Voltage MIC_BIAS_CTRL = 0b		2.5	V
MIC_BIAS_CTRL = 1b			
DC Output Current (I_{OUT}) Per Output		3	mA
Output Resistance (ROUT)		35	ohm
Dropout Voltage		0.34	V
PSRR with 100 mVPP signal AC-coupled to VA supply	217 Hz	105	dB
	1K Hz	100	dB
	20 KHz	90	dB
PSRR with 100 mVPP signal AC-coupled to VP supply	217 Hz	90	dB
	1K Hz	90	dB
	20 KHz	70	dB